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2.5(RR) 2.5(R)(1arm&LHF) 1.5S No Arm 2.5S No Arm 3(RR) 3(R ...

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1 Arm J1:1 - A518 (W) T Arm J1:2 - A518 (E) - Straight

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ROBOTIC ARM CONTROL THROUGH HUMAN ARM ...

Fig8. Screenshot Of AVR Studio 4 Running On Windows 7 Platform 21 Fig9.

Screenshot Of SinaProg 2.0 Running On Windows 7 Platform 22 Fig10. Screenshot Of MATLAB V7.6 (R 2012a) Running On Windows 7 Platform 23 Fig11. Block Diagram Of 16th, 2024

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0 5 10 15 20 25 30 35 40 1 2 4 MIPS Number Of Cores (Instruction Set Simulators) Avg. ISS MIPS Acc. System MIPS 3 VP Simulation Performance N Example: UC/MC VP Performance (MIPS)-Target SW: COREMARK/Linux-Test Single/dual/quad Core Systems-In-house Instruction Set Simulator (ISS)-OSCI/Accellera1SystemC KernelReduced Simulation 1th, 2024

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