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1 Arm J1:1 - A518 (W) T Arm J1:2 - A518 (E) - Straight

Arm J1:1 - A518 (W) 1 Arm J1:2 - A518 (E) - Straight 1 P 1) 1 2 B B 1 T) 1 T 1 T 1 A B C. Full Input Data And Results . Network

Results . Item Lane Description Lane Type Controller Stream Position In Filtered Route Full Phase May 15th, 2024

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0 5 10 15 20 25 30 35 40 1 2 4 MIPS Number Of Cores (Instruction Set Simulators) Avg. ISS MIPS Acc. System MIPS 3 VP Simulation Performance N Example: UC/MC VP Performance (MIPS)-Target SW: COREMARK/Linux-Test Single/dual/quad Core

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Bolton, G. (2010). Reflective Practice: Writing And Professional Development. London: Sage Publications Ltd. Gillie Boltonová

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