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In A Parallel Form (to A PCI-DIO-32HS Digital I/O Card) Or Alternatively Back To LVDS. The LVDS Output Could Then Be Further Post-processed, For Example, In A Correlator. This Type Of Post-processing Architecture Could Possibly Be Implemented In A EP20K-160EQC208-1 Altera FPGAs (\$250 Each) Depending On The Desired Functionality. This Jan 8th, 2024

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