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Will Release The Local Bus During T4 Of The Cycle When All The Following Conditions Are Met: 1.Request Occurs On Or Before T2. 2.Current Cycle Is Not The Low Byte Of A Word (on An Odd Address). 3.Current Cycle Is Not The First Acknowledge Of An Interrupt Acknowledge Sequence. 4.A Locked Instruction Is Not Currently Executing. Mar 8th, 2024

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Author(S) Yu-Cheng Liu Glenn A. Gibson.. Microcomputer Systems-The 8086 / 8088 Family - Y.C. Liu And G. A. Gibson - Microcomputer Systems-The 8086/8088 Family : Architecture, Programming And Microcomputer Systems-The 8086/8088 Family : Architecture, Programming And Design 2nd Edition, Authored By Glenn A. Gibson And Apr 17th, 2024

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•Write Line Indicates 8086/8088 Is Outputting Data To A Memory Or I/O Device. -during The Time WR Is A Logic 0, The Data Bus Contains Valid Data For Memory Or I/O -high-impedance During A Hold Acknowledge INTA •The Interrupt Acknowledge Signal Is A Response To The INTR Input Pin. -normally Used To Gate The Interrupt Vector Number Mar 17th, 2024

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Microcomputer Systems The 8086/8088 Family Architecture Programming And Design Author (S) Yu-Cheng Liu Glenn A. Gibson Publication Data Englewood Cliffs: Prentice Hall Publication€ Date 1986 Edition € 2nd.ed Physical Description IX, 623p Subject Computer Subject Headings Microcomputers Intel 8086 Microprocessor Intel 8088 Microprocessor. May 7th, 2024

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